REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 3, 5-7, 11, and 23 have been amended. Claims 2, 4, and 13-22 were previously canceled. No new matter has been added. Thus, claims 1, 3, 5-12, and 23 are currently pending in this application and subject to examination.

I. Allowable Subject Matter

The Applicants thank the Examiner for the allowance of claims 6-12.

II. 35 U.S.C. § 112

In the Office Action mailed August 29, 2006, Claims 1, 3, and 23 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claims 1, 3, and 23 have been amended responsive to this rejection.

A. Claim 1

The Office Action asserts that claim 1 is indefinite because the recitation "wherein the counter is a counter for obtaining the count value by counting the number of the effective transition edges of the input clock signal, existing during the counting period when the reference clock signal is only at a High level" is misdescriptive because Figures 3 and 4 show that the counter continuously counts regardless of the level High or Low of the reference clock signal.

In describing Figure 4, the Office Action describes the counting cycle as changing from 1 to Nv. The Office Action appears to be referring to Figure 4 of U.S. Patent No. 5,982.208 to Kokubo ("Kokubo") and not Figure 4 in the present application

because Figure 4 in the present application does not depict a count value from 1 to Nv, the present application merely shows the count value as CN1, CN2. Kokubo shows a counted value ranging from 1 to Nv.

Claim 1 corresponds to an embodiment shown in Figures 2 and 3, but <u>not</u> Figure 4. Figure 4 shows an embodiment corresponding to claim 23. Figure 5 shows an embodiment corresponding to claim 3. The table below shows the relationship between the embodiments depicted in Figures 2-5, and the claims.

<u>Claim</u>	**<u>Figure Corresponding to Claim</u>**
1	2, 3
3	2, 5
23	2, 4

Claim 1 has been amended to recite "a counter for delivering a <u>total</u> count value by counting the <u>total</u> number of effective transition edges of the output clock signal, existing . . . during the counting period when the reference clock signal is only at a High level " in order to clarify that the recited count value is not an internal sequential count value, but a total count value for the counting period.

i. <u>Function and Output of a Common Counter</u>

A counter generally has an internal count value (e.g. 1, 2, 3, . . .) with respect to an input signal (e.g. effective edge) after reset. However, the counter does not always output this internal value directly. Specifically, even if the number of effective edges of the input signal is counted and the internal value is sequentially incremented, the counter may continuously output a constant value (e.g. a total count value) which is a

finally obtained value (the total number of effective edges) during a counting period. The counter would output this constant value after the expiration of the counting period.

This is the type of counter that is used in the invention recited in claim 1. Figure 3 shows that the counter 2 outputs a constant count value CN (CN1, CN2) corresponding to the total count value recited in claim 1 in sync with an output clock signal ST after expiration of the counting period (the High level period T1 in the embodiment shown in Figure 3).

Additionally, in such a counter, the processing made when the input signal is input during a non-counting period may include several patterns. For example, the counter may be interrupted to count the internal value during the non-counting period. In another example, the counter may be caused to count the internal value even during the non-counting period, but reset the internal value immediately after the start of the counting period to prevent influences of the input signal input during non-counting periods from affecting the internal value and the total count value during the counting period. Regardless of the type of processing that occurs outside of the counting period, in claim 1, the counter outputs the total count value, obtained during the counting period, as a constant value until the end of the next counting period. This is not related to how the processing is actually performed during the non-counting period. It is only essential that the processing outside the counting period not affect the total count value during the counting period.

Thus, in claim 1, while the counter has an internal count that increases sequentially during a counting period until the counter is reset, the counter only outputs the total count value (CN) after the expiration of the counting period. The counter

maintains the output of the total count value (CN1) as a constant value until the end of the next counting period, at which it outputs the next total count value (CN2) as a constant value, and so forth.

ii. Antecedent Basis

The Office Action asserts that "the counting period" on lines 14-15 lacks antecedent basis. The Applicants respectfully submit that "the counting period" has antecedent basis in "a predetermined counting period" on lines 5-6 of claim 1.

For all of the above reasons, the Applicants submit that claim 1, as amended, is definite.

B. Claim 3

Claim 3 has been amended responsive to the rejection. Claim 3 now recites "the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal."

The Office Action asserts a rejection of claim 3 similar to claim 1 with regard to the count value. For similar reasons to those discussed above for claim 1, the Applicants submit that claim 3, as amended to recite "a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal" is definite.

Furthermore, as mentioned above with reference to claim 1, the Office Action refers to Figure 4 in describing claim 3, yet describes Figure 4 of Kokubo rather than Figure 4 of the present invention.

C. Claim 23

Claim 23 has been amended responsive to the rejection to clarify that the counter delivers "a total count value by counting the total number of effective transition edges of the output clock signal." The Office Action asserts that claim 23 is misdescriptive because it recites that the counter delivers a count value by counting the effective transition edges when the reference clock is only at a Low level. The Office Action asserts that ST is the output of the counter. However, the Applicants submit that ST is the output clock signal not the output (CN) of the counter 2. The counter counts transitions of the output clock signal (ST) during a counting period and outputs a total count value for the counting period.

Claim 23 has been amended to clarify that the counter delivers a "total count value" rather than a sequentially increasing count number internal to the counter.

As discussed above, the counter internally keeps counting the number of effective transition edges of the output clock signal (ST) during a predetermined counting period. However, the counter only delivers a total count value (CN) which is maintained at a constant value until the end of the next counting period. This is shown in Figure 4 of the present application, where the count value CN1 is maintained at a constant value until the end of the counting period T2, when it is replaced by the total count value CN2.

For the above reasons, the Applicants submit that claim 23 is definite and respectfully request the withdrawal of the rejection of claims 1, 3, and 23.

III. 35 U.S.C.§ 102

Claims 1, 3, 5, and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,982,208 to Kokubo et al. ("Kokubo"). It is noted that claims 1, 3, 5, and 23 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection as follows.

A. Counter in the Present Invention and Kokubo

As described above in connection with the rejections under 35 U.S.C. § 112, the claims have been amended to clarify that the counter 2 of the present invention output the total count value CN (e.g. CN1, CN2) as shown in Figures 2 and 3. The counter 5 of Kokubo similarly outputs a count value Nv as shown in Figure 11. Neither counter outputs an intermediate value (e.g. 1, 2, 3 . . .) in counting. The intermediate value is merely an internal count within the counter which counts the output clock signal (ST in the present invention, and fout in Kokubo) input to the counter. The intermediate value is not output from the counter.

Kokubo clearly describes this in Kokubo column 4, lines 7-8. (C) is merely the count value in the counter 5, which increments by one at each cycle of the output clock signal (fout). This is the internal count. However, the count value that is output is Nv, the "current count value" when a gate signal (B) turns to High. Then, the internal count value inside the counter is reset. In other words, the counter 5 does not output the value 1, 2, 3, . . . but outputs only the count value (Nv) at the timing of the gate signal (B) turning to High.

If the counter 5 of Kokubo output the count value 1, 2, 3, . . .as stated by the Office Action, the frequency of the output clock signal (fout) would gradually change as

the counter output the value 1, 2, 3, . . . throughout the period including a High and Low level of the reference clock. When the reference clock returned to a Low level, namely when the output Nv of the counter 5 becomes equal to 1, the frequency of the output clock (fout) in Kokubo would return again to an original frequency.

Thus, if the counter of Kokubo output an incremental count, Kokubo would be a circuit that repeats a frequency sweep of the output clock signal (fout) every counting period. However, Kokubo teaches a clock multiplication circuit that generates an output clock signal having a frequency of a predetermined multiplication of the reference clock signal period. Kokubo does not teach a circuit causing a frequency sweep.

In this regard, the counter of the present invention similarly outputs a total count value CN (e.g. CN1, CN2) rather than outputting an intermediate, internal count number (1, 2, 3 . . .). If the output count value continuously changed from 0 to CN1 during one counting period, the frequency of the output clock signal outputted from VCO would also changed during one counting period and, thus, be periodically repeated. Such a configuration is completely different than the structure described in the present application and claims. As noted above, the claims have been amended to clarify that the counter 2 of the present invention outputs a <u>total</u> count value CN obtained during a counting period rather than an incrementally increasing internal count number.

B. <u>Claim 1</u>

Applicants' invention, as set forth in claim 1, is directed to a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit including a counter for delivering the total count value by counting the total number of

effective transition edges of the output clock signal existing during the counting period when the reference clock signal is only at a High level and the frequency of the output clock signal is changed during a period in which the clock signal is at low level, after the end of the counting period and before the start of a succeeding counting period.

The invention, as claimed in claim 1, allows the frequency clock signal to be maintained at a particular frequency during the next counting period, which suppresses jitter.

In contrast, Kokubo teaches, as shown by line (C) in Figures 4 and 11 of Kokubo, counting (1, 2, 3, . . . Nv) during a period of both a Low and a High level of the reference clock signal (fref) shown by line (A). The counter outputs the count value Nv from its internal counter when the reference clock signal changes from High to Low. If this count value is different from a previously outputted count value, then the frequency of the output clock signal (fout) of VCO1 changes through ACC.REG 18, DAC 9, and LPF 4.

In Kokubo, not only does the counting period correspond to a period of both a Low and a High level of the reference clock signal (fref), but Kokubo also fails to disclose how fast an analog control signal (Vr) and the output clock signal (fout) are generated. Even if such a change is rapid, the change certainly occurs after the time that the level of the reference clock signal (fref) turns from High to Low.

Thus, in Kokubo, the frequency of the output clock signal (fout) output from VCO1 changes during the next counting period (the next period of both a Low and a High level). This change will influence the number of output clock signals (fout) counted during that next period. Therefore, it is impossible to restrain jitter in Kokubo.

In contrast, the clock multiplication circuit set forth in claim 1 has a counting period T1, T2 only during the High level of the reference clock signal (SR), as shown in Figure 3. The circuit of the present invention counts an internal count number within the counter 2, but only the total count value (CN) is output by the counter, as shown in Figure 2 and Figure 3.

In the present invention, the output clock signal (ST) is input to the counter 2 even during non-counting periods (when the reference clock signal (SR) is at the Low level), as noted by the Office Action. However, there is no restriction in claim 1 placed on how the internal counter operates during this period (the non-counting period). There is no limitation on whether or not the internal counter operates during the non-counting period. This is because the value of the internal counter may be reset at the start of the counting period or the internal counter may be restarted, etc. Claim 1 is directed to counting the total number of effective transition edges of the output clock signal (ST) appearing during the counting period in which the reference clock signal is at a High level.

In claim 1, the counter outputs the total count value CN after the expiration of the counting period T1, when the level of the reference clock signal (SR) changes from High to Low. Then, a differential value DN1, an integrated value IN1, and an analog control voltage AV1 are generated in order, and this analog control voltage AV1 is input to VCO7. If the total count value CN1 is different from the previous value, which presents that the analog control voltage AV1 is different from the previous value, the frequency of the output clock signal (ST) output from VCO7 changes.

In the invention set forth in claim 1, the processing of the differential value, integrated value, analog control voltage, and any change in the output clock signal occurs after the counting period (High level period) and before the start of the next counting period (the next High level period). Thus, the frequency change of the output clock signal occurs during the non-counting period (Low level) and will have no influence on the total count value CN2 of the output clock signal (ST) counted by the counter 2 during the next counting period (next High level period). (See Figure 3 showing the frequency of ST changing before the start of the next counting period T2 and remaining unchanged during the counting period T2).

Thus, in the invention recited in claim 1, even when the output clock signal frequency changes, it will not influence the total count value. This restrains jitter. As described above, the count value of Kokubo is influenced by any changes in frequency of the output clock signal, making it impossible to restrain jitter. Thus, the invention set forth in claim 1 provides improved stability of operation.

Kokubo does not disclose or suggest at least the feature of counting the number of effective transition edges of the output clock signal existing during the counting period when the reference clock signal is <u>only</u> at a High level, as recited in claim 1.

The Applicants note that in the rejection under 35 U.S.C. § 112, the Office Action noted the inconsistency between Figure 4 of Kokubo and claim 1.

For at least these reasons, the Applicants submit that claim 1 is allowable over the cited art.

C. Claim 3

Applicants' invention as set forth in claim 3 is directed to a clock multiplication circuit including in part a counter for obtaining the total count value at the end of each High level period and each Low level period of the reference clock signal, in which when the total count value obtained by counting during a High level period of the reference clock signal is changed from a preceding total count value, the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal and in which when the total count value obtained by counting during a Low level period of the reference clock signal is changed from a preceding total count value, the frequency of the output clock signal is changed after the end of the Low level period and before the start of the next Low level period.

In contrast, in Kokubo, one counting period (shown as (B) in Figure 4 of Kokubo), is an entire cycle of the reference clock signal fref (A), including both a High and a Low level period of the reference clock signal rather than having a counting period for each High and each Low level period, as recited in claim 3. The count value in Kokubo (Nv) is obtained only once during the continuous High and Low level period, as shown in (C). (As discussed above, Kokubo only outputs one count value Nv rather than a sequentially increasing internal count number inside the counter 5. See column 4, lines 7-12 of Kokubo.)

In Kokubo, after the counting period, the analog control signal (Vr) changes and the frequency of the output clock signal (fout) of VCO1 changes. At this time, the next counting period has already started, so that the counter has started to count a count

value of the internal counter (e.g. 1, 2, 3, . . .). Thus, the frequency change in the output clock signal (fout) in Kokubo changes during the next counting period and influences the total count value in this counting period. This influence will further affect the frequency in the next counting period. In this way, the influence will affect the subsequent counting periods in sequence and cannot prevent jitter.

In contrast, claim 3, as depicted in Figure 5, includes a counting period (T1, T2, T3, T4) for each high level period and each low level period of the reference clock signal.

In Kokubo, one total count value is obtained during both a Low and a High level period. In claim 3, a total count value is obtained for each Low level period and each High level period, separately, which provides the total count value at a double frequency.

Beyond providing a total count value at double the frequency of Kokubo, the invention recited in claim 3 is also configured to cause a change in frequency of the output clock signal in response to the counter 2, subtracter 3, accumulator 5, DA converter circuit 6, and VCO 7 due to a total count value during a High level counting period (T1) to occur before the start of the next High level counting period (T3). This allows the prevention of the change in frequency from exerting an effect on the total count value CN3 during the counting period T3 two periods later, even if it influences the total count value CN2 during the counting period T2, which is the next counting period (a Low level counting period). By restricting the influence of the change of the frequency of the output clock signal within a predetermined range, it is possible to

restrain jitter from occurring in the frequency of the output clock signal ST of the circuit in claim 3.

Therefore, the Applicants submit that Kokubo does not disclose or suggest a clock multiplication circuit , in which at least when the total count value obtained by counting during a High level period of the reference clock signal is changed from a preceding total count value, the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal and the characteristics in which when the total count value obtained by counting during a Low level period of the reference clock signal is changed from a preceding total count value, the frequency of the output clock signal is changed after the end of the Low level period and before the start of the next Low level period.

The Applicants note that in the rejection under 35 U.S.C. § 112, the Office Action noted the inconsistency between Figure 4 of Kokubo and claim 3.

For at least these reasons, the Applicants submit that claim 3 is allowable over the cited art.

D. Claim 5

Applicants' invention as set forth in claim 5 is directed to a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted wherein a counter delivers a count value after the end of a counting period and in synchronization with an output clock signal, a subtracter generates a difference value in sync with an output clock signal generated after the counter generates a count value in sync with an output clock signal,

a control voltage generation circuit generates an analog control signal in sync with an output clock signal generated after the subtracter generates the difference value in sync with the output clock signal.

Kokubo teaches a clock multiplication circuit and teaches a SUBTRACTOR 17, ACC.REG 18, DAC 9, and LPF 4. However, Kokubo does not disclose or suggest that these elements operate in sync with the output clock signal fout, as recited in claim 1. Kokubo actually depicts these elements as being without input from the output clock signal.

In Figure 11 of Kokubo, the output clock signal (fout) from VCO1 is merely input to the counter 5 and the frequency divider 2. It is not input to SUBTRACTOR 17, ACC.REG 18, and DAC 9. Thus, from the depiction in Figure 11 of Kokubo, the SUBTRACTOR 17, ACC.REG 18, and DAC 9 do not operate in sync with the output clock signal (fout).

The Office Action uses the language of claim 5, asserting that the elements of Kokubo operation "in sync" with the output clock signal. However, the Office Action does not point to any section of Kokubo that discloses or suggests that the elements operate "in sync" with the output clock signal.

The invention recited in claim 5 is depicted throughout Figures 2-5 of the present application. Figure 3 shows the counter 2 outputting the total count value CN1, CN2 in sync with the output clock signal ST. The subtracter 3 outputs a difference value DN1, DN2 in sync with the output clock signal ST after output of the total count value CN1, CN2. Further, a control voltage generating circuit 4 outputs an analog control signal AV1, AV2 in sync with the output clock signal ST after output of the difference value

DN1, DN2. The same applies to Figure 4 and 5 of the present application. Thus, it is possible to change the frequency of VCO7 at a predetermined timing.

Kokubo does not disclose or suggest that the total count value CN1, CN2; difference value DN1, DN2; and analog control signal AV1, AV2 are sequentially made synchronous with the output clock signal ST.

Thus, Kokubo does not disclose or suggest a clock multiplication circuit wherein a counter delivers a count value after the end of a counting period and in synchronization with an output clock signal, a subtracter generates a difference value in sync with an output clock signal generated after the counter generates a count value in sync with an output clock signal, a control voltage generation circuit generates an analog control signal in sync with an output clock signal generated after the subtracter generates the difference value in sync with the output clock signal, as recited in claim 5.

For at least these reasons, the Applicants submit that claim 5 is allowable over the cited art.

E. Claim 23

The Applicants' invention as set forth in claim 23 is directed to a clock multiplication circuit including, in part, a counter for delivering a total count value by counting the total number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a low level and the frequency of the output clock signal is changed during a period in which the reference clock signal is a High level, after the end of the counting period and before the start of a succeeding counting period.

Claim 23 is directed to an invention that can be generalized as a reverse of claim 1. Claim 23 is directed to an embodiment of the invention depicted in Figure 4 of the present application.

The Office Action asserts that the count value of Kokubo changes from Nv-2 to Nv. The Applicants agree that the internal count number inside of the counter 5 in Kokubo changes incrementally. However, as described above, Kokubo teaches that only the value Nv is output to the comparator when signal (B) goes to a high level. (See Kokubo column 4, lines 7-13). Thus, although Figure 4 of Kokubo shows the internal count number within the counter (C) changing from Nv-2 to Nv during the High level period of the reference clock signal, Nv-2 and Nv-1 are not the "total count value" "delivered" by the counter, as recited in claim 23. Thus, in Kokubo, the frequency of the output clock signal (fout) of VCO1 will not change when the internal count number within the counter change from Nv-2 to Nv.

As discussed above for claim 1, Kukobo teaches both a high and a low level as one counting period and the output clock signal being changed during following counting period, which makes it impossible to suppress jitter.

Thus, the Applicants submit, that Kukobo fails to disclose or suggest a clock multiplication circuit including at least the features of a counter for delivering a count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a low level and the frequency of the output clock signal is changed during a period in which the reference clock signal is a High level, after the end of the counting period and before the start of a succeeding counting period, as claimed in claim 23.

For at least these reasons, the Applicants submit that claim 23 is allowable over the cited art.

CONCLUSION

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, with reference to Attorney Docket No. 024016-00063.

Respectfully submitted,

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